

Manual

IF2008A PCI Basis Board
IF2008E Expansion Board

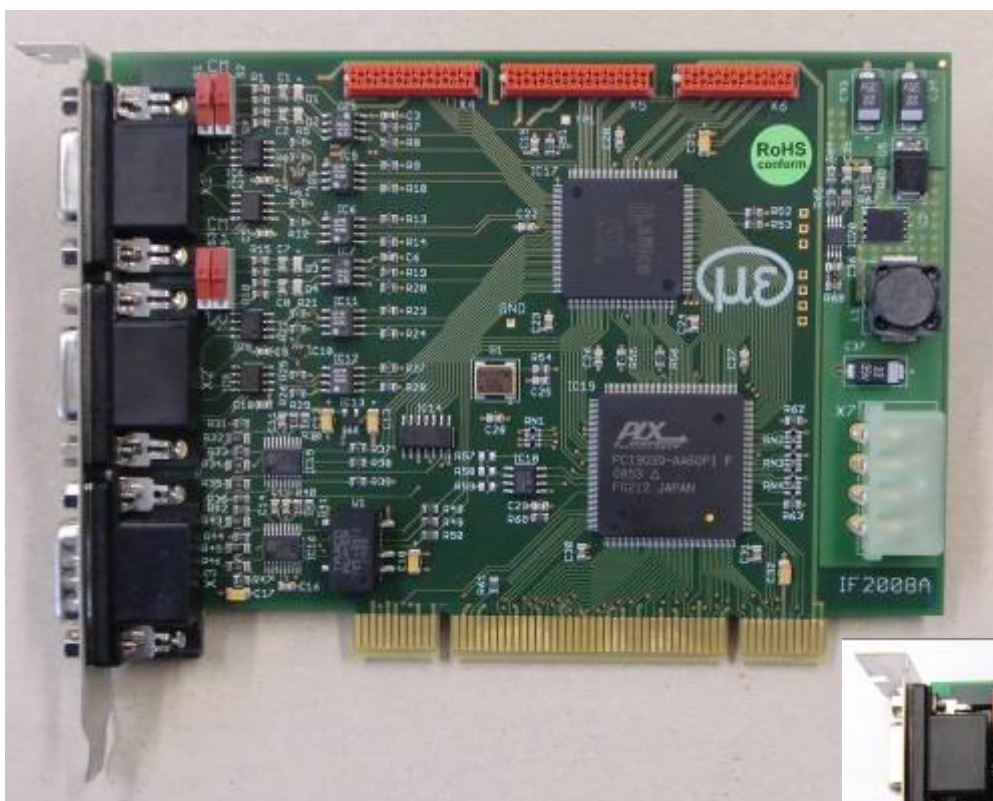


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1 Technical Data

1.1 IF2008A Basic Printed Circuit Board

Mechanics and Environment

- Dimensions (circuit board) approx. 140 x 102 mm, 1 slot wide
- Ambient temperature +50°C maximum
- 2x D-SUB female connectors HD 15-pin for sensor connections
- 1x D-SUB male connector HD 15-pin for encoder signals
- Tyco/AMP Commercial MATE-N-LOK connector (IDE hard drive connector) for supply DC-/DC converter
- 3x female connectors Tyco/AMP MicroMatch for connection to IF2008E

PCI-Bus

- PCI connector 3.3 or 5 Volt 32 bit 2x60 pin
- Target interface (slave) according to specifications Rev. 2.1 and 2.2
- Bus clock frequency 40 MHz maximum
- Current consumption +5 Volt approx. 0.5 A, sensors and encoder excluded

Sensor Interface (X1 / X2)

- 2 RS422 driver and two RS422 receiver including galvanic isolation per connector (in- / output frequency 5 MHz maximum)
- 2 LVDS or 3.3 Volt CMOS outputs including galvanic isolation per connector (output frequency 5 MHz maximum)
- Power supply of the sensors 24 V

Encoder Interface (X3)

- Interface for two encoders with 1 V_{ss} , RS422- (differential-) or TTL- (single-ended) signals
- Power supply of the encoders with +5 V, PCI supply without galvanic isolation (current consumption depends on encoders connected)
- Interpolation programmable from 1- to 64 times in case of encoders with 1 V_{ss} signals (input frequency maximum = $[3.2 \text{ MHz} / \text{interpolation}] \leq 800 \text{ kHz}$)
- Evaluation programmable from 1- to 4-times in case of encoders with:
 - RS422- / differential signal (input frequency max. = 800 kHz)
 - TTL- / single-ended signals (input frequency max. = 400 kHz)

DC-/DC-Converter

- Input voltage range 12 V \pm 1.0 V
- Output voltage 24 V \pm 0.5 V
- Output current 1.25 A max. for all sensors
- Efficiency typical 90 %

The supply of the DC-DC converter with power supply within the computer. The connection between the PC power supply and the IF2008A has to be done during the installation of the card.

1.2 IF2008E Expansion Board

Mechanics and Environment

- Dimensions (conductor board) approx. 71 x 102 mm, 1 slot wide
- Ambient temperature +50 °C maximum
- 1x D-SUB female connector HD 15-pin for sensor connections
- 1x D-SUB female connector 9-pin for I/O-Interface
- 1x D-SUB male connector 9-pin for analog inputs
- 3x female connectors MicroMatch for connection to IF2008A

Sensor Interface (X1)

- Similar to IF2008A (X1)

I/O Interface (X2)

- 4 optocoupler inputs, current input 5 mA maximum, input frequency 1 MHz maximum
- 4 optocoupler outputs, current output 20 mA maximum, output frequency 1 MHz maximum

Analog Interface (X3)

- 2x ADC channels
- Input voltage range 0-5 V, 0-10 V, ± 5 V, ± 10 V adjustable separately for each channel by means of DIP switch
- Resolution 16 bit
- Offset error ± 3 mV maximum
- Gain error ± 5 mV maximum
- Conversion rate 150 kHz maximum per channel

2 Hardware

2.1 View IF2008A

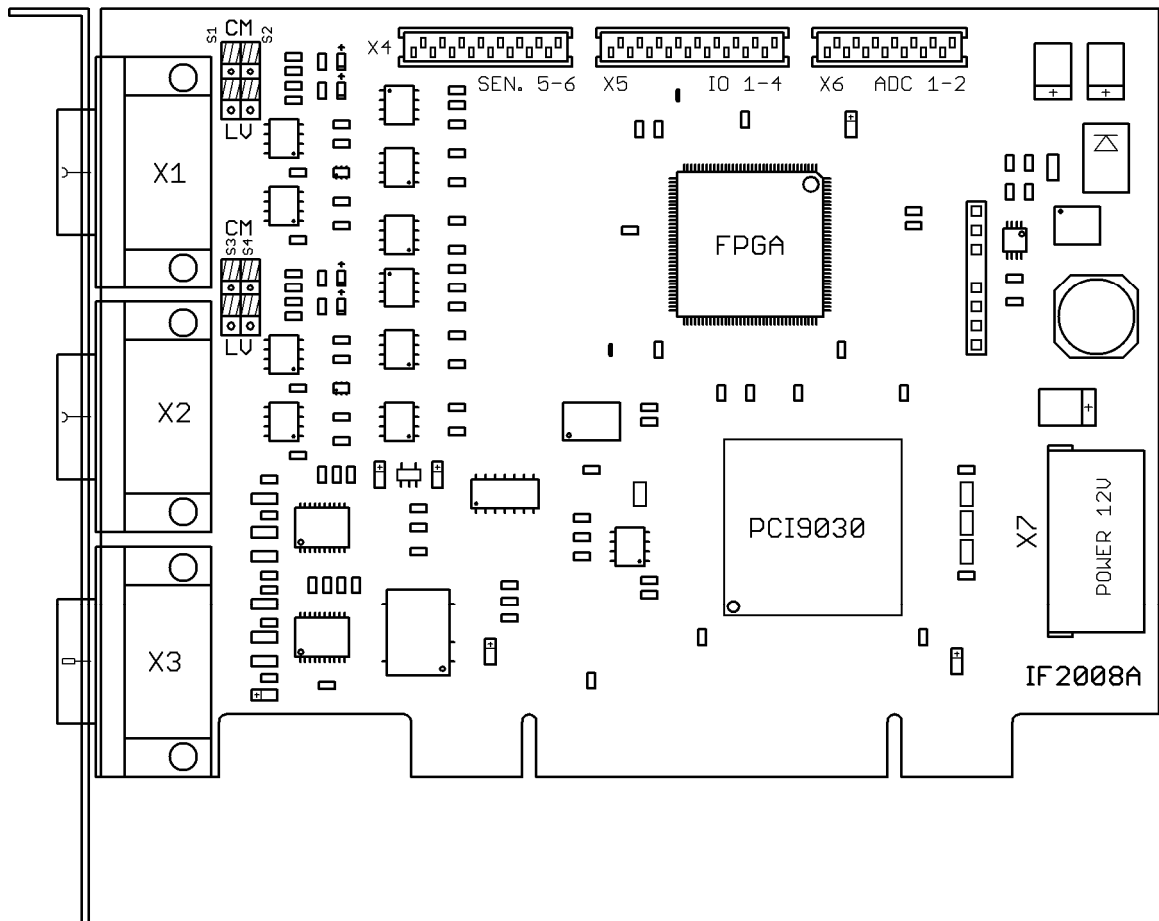


Image 1: View of board IF2008A

- X1 = Sensor connection 1 and 2
- X2 = Sensor connection 3 and 4
- X3 = Encoder connection 1 and 2
- X4 ... X6 = Connection to IF2008E
- X7 = Connection 12 V power, connection to the power supply required
- S1 .. S4 = Switch for positive trigger level

2.2 View IF2008E

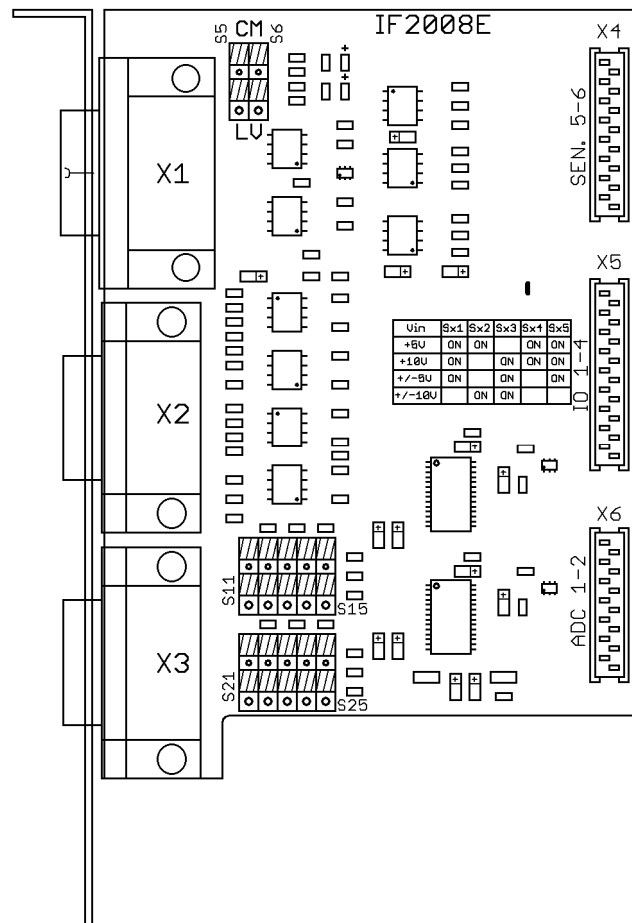


Image 2: View of board IF2008A

- X1 = Sensor connection 5 and 6
- X2 = Connection for I/O signals
- X3 = Connection to analog digital converter
- X4 ... X6 = Connection to IF2008A
- S5 u. S6 = Switch for positive trigger level
- S11 ... S15 = Switch for ADC level 1
- S21 ... S25 = Switch for ADC level 2

3 Pin Assignments and Jumper Setting

3.1 Sensor Interface (IF2008A X1 and X2, IF2008E X1)

Pin	Signal
1	Sensor 1 TxD-
2	Sensor 1 TxD+
3	Sensor 1 RxD-
4	Sensor 1 RxD+
5	Power supply 0V
6	Sensor 1 TRG+
7	Sensor 1 TRG-
8	Sensor 2 TRG+
9	Sensor 2 TRG-
10	Power supply +24V
11	Sensor 2 TxD-
12	Sensor 2 TxD+
13	Sensor 2 RxD-
14	Sensor 2 RxD+
15	GND (galvanic isolation to PC-GND)

Table 1: Pin assignment sensor interface

3.2 Encoder Interface (IF2008A X3)

Pin	Function
1	Encoder 1 track A+
2	Encoder 1 track A-
3	Encoder 2 track A+
4	Encoder 2 track A-
5	VCC (+5V)
6	Encoder 1 track B+
7	Encoder 1 track B-
8	Encoder 2 track B+
9	Encoder 2 track B-
10	GND
11	Encoder 1 track R+
12	Encoder 1 track R-
13	Encoder 2 track R+
14	Encoder 2 track R-
15	GND

Table 2: Pin assignment encoder interface

Attention: The pin assignment is not compatible with IF2004B!

3.3 Sensor Power (IF2008A X7)

Pin	Function
1	+12 V
2	GND
3	GND
4	NC

Table 3: Pin assignment sensor power

3.4 I/O Interface (IF2008E X2)

Pin	Function
1	OUT 1
2	OUT 2
3	OUT 3
4	OUT 4
5	GND (galvanic isolation to PC-GND)
6	IN 1
7	IN 2
8	IN 3
9	IN 4

Table 4: Pin assignment I/O interface

3.5 Analog Interface (IF2008E X3)

Pin	Function
1	Input signal 1
2	Analog GND
3	Input signal 2
4	Analog GND
5	NC
6	NC
7	NC
8	NC
9	NC

Table 5: Pin assignment analog interface

3.6 Jumper-/Switch Setting for Trigger Level

By means of the switches S1 to S4 (IF2008A) and the switches S5 and S6 (IF2008E) the positive trigger level for the sensor channels 1 to 4 (IF2008A) or 5 and 6 (IF2008E) can be selected. The negative output always has LVDS level.

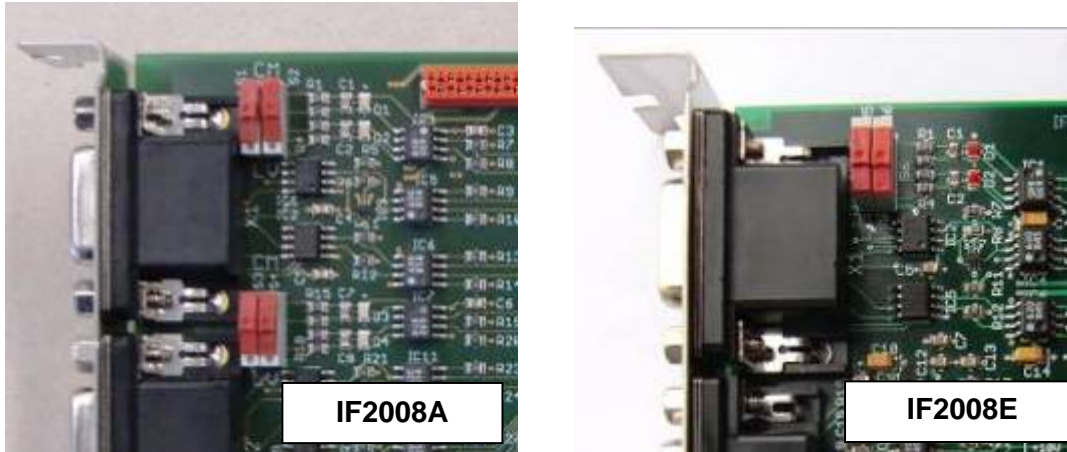


Image 3: Switch settings trigger level

Switch	Setting	Trigger output +
S1 to S6	CMn	3.3 V CMOS level for sensor n TRG+
	LVn	LVDS level for sensor n TRG+

Table 6: Switch settings trigger level

3.7 Switch Settings for ADC Level

By means of the switches S11 to S15 and S21 to S25 the input voltage range of the analogue-digital converter for the sensor channel 5 and 6 on the IF2008E can be selected.

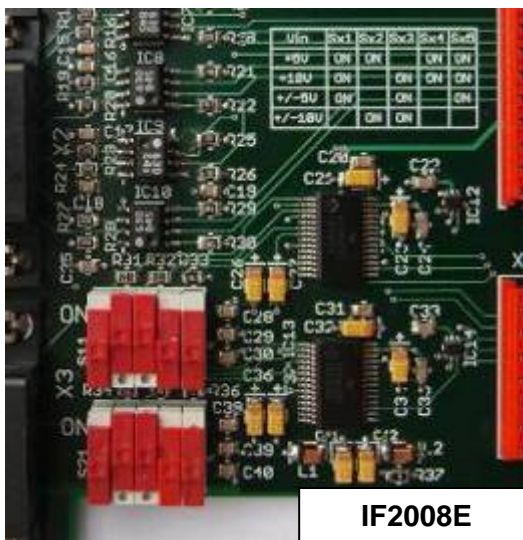


Image 4: Switch settings ADC level
(Settling in the image ± 10)

VIN	Sx1	Sx2	Sx3	Sx4	Sx5
0-5 V	ON	ON		ON	ON
0-10 V	ON		ON	ON	ON
± 5 V	ON		ON		ON
± 10 V		ON	ON		

Table 7: Switch settings ADC level

Setting
ON
OFF

4 Address Assignment

4.1 PCI Interface

Interface: 16 bit PCI bus with 3.3 or 5 Volt connection

Access: Memory space 40 Hex addresses

Base address: Automatic allocation by operating system

Header Configuration

Addr.	Byte 3	Byte 2	Byte 1	Byte 0	Value (Hex)
00h	Device ID		Vendor ID		9030 10B5
18h	Base address local memory space				xxxx xxxx
2C	Subsystem ID		Subsystem Vendor ID		2302 2810

Table 8: Header configuration

4.2 Local Address Assignment

Base addr. +	Write Access	Read Access
00h	Transmit register	FIFO data
02h	Set / reset / latch register	FIFO volume
04h	FIFO enable register	FIFO Enable register
06h	Interrupt enable register	Interrupt state register
08h	Sensor 1 baud rate	remarked
0Ah	Sensor 2 baud rate	remarked
0Ch	Sensor 3 baud rate	remarked
0Eh	Sensor 4 baud rate	remarked
10h	Sensor 5 baud rate	remarked
12h	Sensor 6 baud rate	remarked
14h	Counter control register 1	Counter control register 1
16h	Counter control register 2	Counter control register 2
18h	Counter 1 preload LSW	Counter 1 LSW
1Ah	Counter 1 preload MSW	Counter 1 MSW
1Ch	Counter 2 preload LSW	Counter 2 LSW
1Eh	Counter 2 preload MSW	Counter 2 MSW
20h	Timer 1 frequency	ADC 1
22h	Timer 1 pulse width	ADC 2
24h	Timer 2 frequency	State
26h	Timer 2 pulse width	Input
28h	Timer 3 frequency	remarked
2Ah	Timer 3 pulse width	remarked
2Ch	Timer Clock divider	Timer Clock divider
2Eh	Output register	Output register
30h	Mode opto- and TxD outputs	Mode opto- and TxD outputs
32h	Mode trigger outputs	Mode trigger outputs
34h	ADC control register	ADC control register
36h	Parity enable register	Parity error

Table 9: Local address assignment

5 Register Description

5.1 Transmit Register

The sending register sends commands to the sensor.

Base addr. + 00h (write access)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			S6	S5	S4	S3	S2	S1	D7	D6	D5	D4	D3	D2	D1	D0
	Selection sensor channel							Data bits								

Table 10: Transmit register

Bit 0 to 7 Include the data for sending register

Bit 8 to 15 Selection sensor channel

Bit 8 = 1 → Data are output on the sensor channel S1

Bit 9 = 1 → Data are output on the sensor channel S2

etc.

Bit 13 = 1 → Data are output on the sensor channel S6

Bit 14..15 → free

Immediately on the write access to the address "0", the data with the bit 8 to 13 selected sensor channel are transmitted. The baud rate for the transmit register is automatically adapted to the selected sensor channel. In case that the data output is effected on more channels, the baud rate of the best channel is used.

5.2 FIFO Data

Answering of the sensor, e.g. measuring values are stored in the FIFO memory and are forwarded to the operator by the functions MEDAQLib.

Base addr. + 00h (read access)

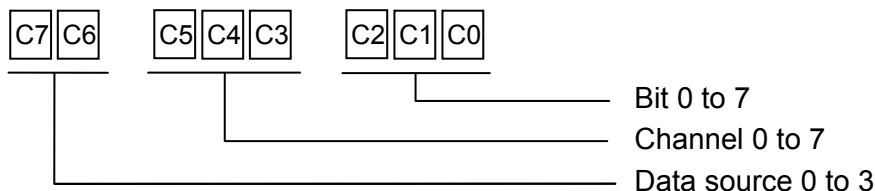
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
	Code bits								Data bits							

Table 11: FIFO Data memory

Bit 0 to 7 Include the data buffered

Bit 8 to 15 Mark the data code

Code bits



C7	C6	Data Source
0	0	Sensor
0	1	Encoder
1	0	Switching input (IN 1..4 → channel 0, RxD 1..6 → channel 1)
1	1	ADC

Table 12: FIFO Data memory – Data sources

5.3 Set- / Reset- / Latch Register

Register to affect the counter.

Base addr. + 02h (write access)

Bit	Function
0	Counter 1 delete, i.e. zeroing with //“Clear_Encoder“
1	Counter 1 load, pre-assigned by a value via //“SetEncoderPreload“ forwarded to the IF2008 via //“Load_Encoder“.
2	Counter 1 latch, get current numeric value
3	Counter 1 reference with //“EnableRef_Encoder“, requires Set_EncoderMode
4	Counter 2 delete
5	Counter 2 load
6	Counter 2 latch
7	Counter 2 reference
8	ADC 1 conversion start, //“Get_ADCValue“ converts and gets a value
9	ADC 1 conversion start
10	FIFO delete with //“Clear_Buffers“.
11 – 15	remarked

Table 13: Set- / reset- / latch register

Please note:

- By means of the bits 0 to 2 and 4 to 6 the counters can be either deleted or loaded independently of the counter control register by the software, (addr. 14h and addr. 16h) Furthermore, the counter reading can be transferred into the latch register.
- If a counter latch or load function, which should only operate in connection with a reference marker signal is settled by the counter control register (addr. 14h and addr. 16h); this is subject to approval by setting bit 3 or bit 7. On setting bit 3 or bit 7 the state bits 0 and 1 or 2 and 3 are reset.
- All bits have to be settled, resetting is not necessary
- In case of power failure all bits are set to "0".
- //“ “ Description of the corresponding commands in the MEDAQLib.

5.4 FIFO Volume

Base addr. + 02h (read access)

Bit	Function
0 to 11	FIFO data volume (0 to 4095)
12 to 15	permanent 0

Table 14: FIFO volume

The dataset is transferred automatically into the FIFO data memory on receipt. By means of a report of the FIFO volume the FIFO data amount can be calculated. The order and speed regarding buffering the data received, is similar to the data stream of the receiving register. In case that the FIFO is not readout quickly enough the latest data (4096) received is available.

Is used by the MEDAQLib internally, there is no individual command.

5.5 FIFO Enable Register

The FIFO-Enable-Register is internally dealt by MEDAQLib.

Base addr. + 04h (write and read access)

Bit	Function
0	0 = FIFO for sensor channel 1 blocked 1 = FIFO for sensor channel 1 released
1	0 = FIFO for sensor channel 2 blocked 1 = FIFO for sensor channel 2 released
2	0 = FIFO for sensor channel 3 blocked 1 = FIFO for sensor channel 3 released
3	0 = FIFO for sensor channel 4 blocked 1 = FIFO for sensor channel 4 released
4	0 = FIFO for sensor channel 5 blocked 1 = FIFO for sensor channel 5 released
5	0 = FIFO for sensor channel 6 blocked 1 = FIFO for sensor channel 6 released
6	0 = FIFO for encoder channel 1 blocked 1 = FIFO for encoder channel 1 released
7	0 = FIFO for encoder channel 2 blocked 1 = FIFO for encoder channel 2 released
8	0 = FIFO for state of external inputs IN 1..4 blocked 1 = FIFO for state of external inputs IN 1..4 released
9	0 = FIFO for state of RxD inputs (sensor 1..6) blocked 1 = FIFO for state of RxD inputs (sensor 1..6) released
10	0 = FIFO for ADC 1 blocked 1 = FIFO for ADC 1 released
11	0 = FIFO for ADC 2 blocked 1 = FIFO for ADC 2 released
12	0 = FIFO in case of active, ext. Input IN 1 for sensor 1 and 2 blocked 1 = IN 1 has no affect on FIFO
13	0 = FIFO in case of active, ext. Input IN 2 for sensor 3 and 6 blocked 1 = IN 2 has no affect on FIFO
14	0 = FIFO in case of active, ext. Input IN 3 for encoder 1 and 2 blocked 1 = IN 3 has no affect on FIFO
15	0 = FIFO in case of active, ext. Input IN 4 for ADC 1/2; IN 1..4; RxD 1..6 blocked 1 = IN 4 has no affect on FIFO

Table 15: FIFO enable register

Data acquisition in blocks. Defines which data e.g. of the sensors will be stored in the FIFO. The FIFO has 4095 bytes. If 2/3 of the capacity in the FIFO are reached, the driver of the IF card evaluates the data of the FIFO and stores them in the driver buffer at a maximum rate of 64kByte. The MEDAQLib gets the data from the driver buffer and stores them in the ring buffer at a maximum rate of 10MByte. Note for bit 9: The RxD inputs can also be used as further control inputs, e.g. of a SPS in the case that the external inputs are not sufficient.

Note for bit 12 to 15: Therefore, the measuring values can either be blocked or evaluated (gating). The command in the MEDAQLib is Use_Gate.

5.6 Interrupt Enable Register

Base addr. + 06h (write access)

Bit	Function
0	1 = Enable interrupt requirements if FIFO more than 50 % reserved
1	1 = Enable interrupt requirements if FIFO more than 75% reserved
2	1 = Enable interrupt requirements on overflow Timer 1
3	1 = Enable interrupt requirements on overflow Timer 2
4	1 = Enable interrupt requirements on overflow Timer 3
5	1 = Enable interrupt requirements if external input IN 1 is activated
6	1 = Enable interrupt requirements if external input IN 2 is activated
7	1 = Enable interrupt requirements if external input IN 3 is activated
8	1 = Enable interrupt requirements if external input IN 4 is activated
9 - 15	remarked

Table 16: Interrupt enable register

The MEDAQLib uses bit 1, more than 75 % of the FIFO is used. The interrupt function enables the data evaluation in the driver buffer.

Please note:

The interrupt generation is controlled by a trigger flange, that means an interrupt requirement is only effected if the corresponding bit is set in the interrupt enable register. Furthermore, the appropriate source has to change from the inactive into the active state. More than one bit can be set at the same time.

5.7 Interrupt State Register

Base addr. + 06h (read access)

Bit	Function
0	1 = Interrupt requirement in case of FIFO level more than 50 %
1	1 = Interrupt requirement in case of FIFO level more than 75 %
2	1 = Interrupt requirement on overflow Timer 1
3	1 = Interrupt requirement on overflow Timer 2
4	1 = Interrupt requirement on overflow Timer 3
5	1 = Interrupt requirements on activating the external input IN 1
6	1 = Interrupt requirements on activating the external input IN 2
7	1 = Interrupt requirements on activating the external input IN 3
8	1 = Interrupt requirements on activating the external input IN 4
9 - 15	remarked

Table 17: Interrupt status register

Enables a report which interrupt has occurred. The MEDAQLib uses bit 1. The register can not be reached from outside, it is only used by the driver.

Please note:

The interrupt state register informs by which source(s) the interrupt requirements have been generated. One interrupt requirement can be effected by using more than one source at the same time. In case that no state bit is set, the interrupt requirement was not generated by the IF2008A but by another hardware.

5.8 Sensor Baud Rate

Base addr.	Sensor Channel	Value	Access
+ 08h	1	1 to 65,535	write access only
+ 0Ah	2	1 to 65,535	write access only
+ 0Ch	3	1 to 65,535	write access only
+ 0Eh	4	1 to 65,535	write access only
+ 10h	5	1 to 65,535	write access only
+ 12h	6	1 to 65,535	write access only

Table 18: Base addresses for sensor baud rates

Depending on the sensor, the register is set automatically. It cannot be reached directly by the operator. In the case of sensors with a variable baud rate, the baud rate can be set while opening the sensor. Additionally, the MEDAQLib sets the corresponding baud rate in the IF card.

$$\text{Value} = (40 \text{ MHz} / \text{Baud rate}) - 1$$

Example:

Requested baud rate = 691.2 kBaud

$$\text{Value} = (40 \text{ MHz} / 691.200) - 1 = 57.87$$

The input value has to be an integer i.e. the result has to be rounded:

$$\rightarrow \text{Value} = 58$$

5.9 Counter Control Register

Base Adr	Counter Channel	Bit	Access
+ 14h	1	0 to 15	write and read access
+ 16h	2	0 to 15	write and read access

Table 19: Base addresses for counter control register

The counter control register states the operating procedure of the encoder.

The labels below are similar to both counter channels!

Functional Overview

Bit	Function
0 to 3	Interpolation (see Table 21: Encoder interpolation) //Set_EncoderInterpolation respectively Get_EncoderInterpolation
4	Direction of counting (see Table 22: Encoder counter direction) //Set_EncoderDirection respectively Get_EncoderDirection
5 to 7	Counter mode (see table 23: counter mode) //Set_EncoderMode respectively Get_EncoderMode
8 to 11	Latch source (see table 24: counter latch source) //Set_EncoderLatchSource respectively Get_EncoderLatchSource
12 to 15	remarked

Table 20: Functional overview for counter control register

Interpolation

Bit 3	Bit 2	Bit 1	Bit 0	Interpolation
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	8
0	1	1	1	10
1	0	0	0	12
1	0	0	1	16
1	0	1	0	20
1	0	1	1	24
1	1	0	0	32
1	1	0	1	40
1	1	1	0	48
1	1	1	1	64

Table 21: Encoder interpolation

Please note:

- for encoders with 1 V_{SS} – signals all interpolations are suitable
- for encoders with TTL – signals the following interpolations are suitable: 1-, 2- or 4-times.
For example 4 times interpolation: In the case of an increasing or falling flank and track A and track B, therefore 4 times of counting pulses.

Counter Direction

Bit 4	Counter Direction
0	usual
1	inverse

Table 22: Encoder counter direction

Counter Mode:

The counter mode sets the operating procedure of the encoder in the case of references.

Bit 7	Bit 6	Bit 5	Counter Mode						
0	0	0	No counter load or delete function by encoder reference marker						
0	0	1	Counter is loaded with the next encoder reference marker as far as the state bit 0 or state bit 2 "0" is settled.						
0	1	0	Counter is loaded including all encoder reference markers and load register content. State bit 0 to 3 are not affected.						
0	1	1	Counter is deleted including all encoder reference markers and additionally loaded with the content of the load register if the counter has reached -1. This function offers the possibility to limit the counter. During this process the counter load register has to be preallocated with the number of increments limited -1.						
1	0	0	Counter excluded phase discriminator (Counter) <table border="1" data-bbox="628 1845 1428 2040"> <thead> <tr> <th>Bit 4</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Track A = counter direction signal Track B = counter clock signal</td> </tr> <tr> <td>1</td> <td>Track A = counter clock signal Track B = counter direction signal</td> </tr> </tbody> </table>	Bit 4	Function	0	Track A = counter direction signal Track B = counter clock signal	1	Track A = counter clock signal Track B = counter direction signal
Bit 4	Function								
0	Track A = counter direction signal Track B = counter clock signal								
1	Track A = counter clock signal Track B = counter direction signal								
1	0	1	remarked						

1	1	0	remarked
1	1	1	remarked

Table 23: Counter

Latch Source:

Enables the synchronised acquisition of the sensor and the encoder values. The command in the MEDAQLib is Set_EncoderLatchSource.

Bit 11	Bit 10	Bit 9	Bit 8	Latch Source
0	0	0	0	Hardware latch blocked
0	0	0	1	Timer 1
0	0	1	0	Timer 2
0	0	1	1	Timer 3
0	1	0	0	Sensor channel 1
0	1	0	1	Sensor channel 2
0	1	1	0	Sensor channel 3
0	1	1	1	Sensor channel 4
1	0	0	0	Sensor channel 5
1	0	0	1	Sensor channel 6
1	0	1	0	IN 1 (IF2008E only)
1	0	1	1	IN 2 (IF2008E only)
1	1	0	0	IN 3 (IF2008E only)
1	1	0	1	IN 4 (IF2008E only)
1	1	1	0	2. reference
1	1	1	1	All reference markers

Table 24: Counter latch source

5.10 Counter Preload

Pre-Assignment register for the encoder starting values, 32 bit wide. The command in the MEDAQLib is Set_EncoderPreload.

Base addr.	Counter Channel	Value	Access
+ 18h	1 LSW	0 to 65,535	Write access only
+ 1Ah	1 MSW	0 to 65,535	Write access only
+ 1Ch	2 LSW	0 to 65,535	Write access only
+ 1Eh	2 MSW	0 to 65,535	Write access only

Table 25: Base addresses for counter preload

5.11 Counter Value

Command for evaluation. The command in the MEDAQLib is Get_EncoderValue.

Base addr.	Counter Channel	Value	Access
+ 18h	1 LSW	0 to 65,535	Read access only
+ 1Ah	1 MSW	0 to 65,535	Read access only
+ 1Ch	2 LSW	0 to 65,535	Read access only
+ 1Eh	2 MSW	0 to 65,535	Read access only

Table 26: Base addresses for counter value

LSW = Least significant word

MSW = Most significant word

5.12 Timer

Command in the MEDAQLib: Set_TimerFrequency.

Application:

- Set Timer to digital output
- Synchronising data acquisition
- Get triggering signal

Example: Time-based synchronising of the sensor using the command Set_TriggerSource.

Base addr.	Timer	Value	Access:
+ 20h	1 frequency	0 to 65,535	Write access only
+ 22h	1 pulse width	0 to 65,535	Write access only
+ 24h	2 frequency	0 to 65,535	Write access only
+ 26h	2 pulse width	0 to 65,535	Write access only
+ 28h	3 frequency	0 to 65,535	Write access only
+ 2Ah	3 pulse width	0 to 65,535	Write access only
+ 2Ch	Clock divider		Write and read access

Table 27: Base addresses for timer

$$\text{Value(F)} = (F_{\text{Clock}} / F_{\text{OUT}}) - 1$$

$$\text{Value(PW)} = (PW_{\text{OUT}} / T_{\text{Clock}})$$

Example:

Requested frequency $F_{\text{OUT}} = 10 \text{ kHz}$

Requested pulse width $PW_{\text{OUT}} = 25 \mu\text{s}$

Clock divider = 0 $\rightarrow F_{\text{Clock}} = 20 \text{ MHz}$, $T_{\text{Clock}} = 50 \text{ ns}$ (clock divider see table below)

$\text{Value(F)} = (20 \text{ MHz} / 10 \text{ kHz}) - 1 = 1999$

$\text{Value(PW)} = (25 \mu\text{s} / 50 \text{ ns}) = 500$

The input values have to be integer!

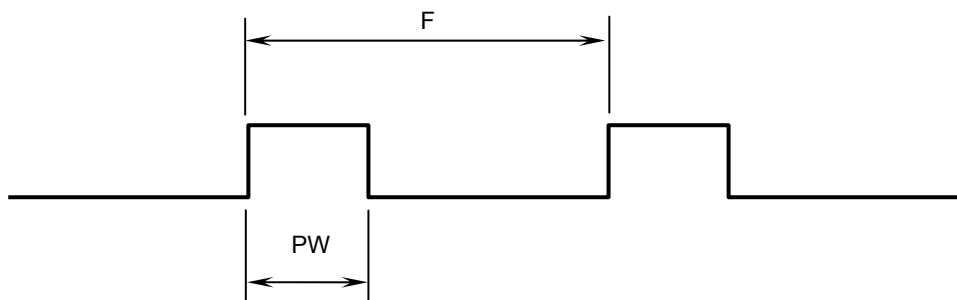


Image 5: Timer frequency and pulse width

Please note:

The pulse width only affects the output “sensor trigger” and “optocoupler”.

The internal synchronization signals are not affected. The timer zero crossing is used.

In order to switch off the timer, the frequency "0" has to be set. If in case of an inactive timer the pulse width is set > 0 , the output is permanently set on high. On the contrary, if the pulse width is set "0", the output is permanently set on low.

Clock Divider:

Bit 3	Bit 2	Bit 1	Bit 0	Clock Frequency Timer 1
Bit 7	Bit 6	Bit 5	Bit 4	Clock Frequency Timer 2
Bit 11	Bit 10	Bit 9	Bit 8	Clock Frequency Timer 3
0	0	0	0	20 MHz
0	0	0	1	20 MHz / 2
0	0	1	0	20 MHz / 4
0	0	1	1	20 MHz / 8
0	1	0	0	20 MHz / 16
0	1	0	1	20 MHz / 32
0	1	1	0	20 MHz / 64
0	1	1	1	20 MHz / 128
1	0	0	0	20 MHz / 256
1	0	0	1	20 MHz / 512
1	0	1	0	20 MHz / 1024
1	0	1	1	20 MHz / 2048
1	1	0	0	20 MHz / 4096
1	1	0	1	20 MHz / 8192
1	1	1	0	20 MHz / 16384
1	1	1	1	20 MHz / 32768

Table 28: Timer clock divider

Please note:

Bit 12 to bit 15 are remarked.

5.13 ADC

Two register for the currently converted values of the A/D converter. MEDAQLib evaluates the values using the command `Get_ADCValue` or by storing them in the FIFO.

Base addr.	ADC Channel	Value	Access
+ 20h	1	0 to 65535	Read access only
+ 22h	2	0 to 65535	Read access only

Table 29: Base addresses for ADC

5.14 State

Base addr. + 24h (read access only)

Bit	Function
0	1 = Encoder 1: 1. reference markers crossed //Get_EncoderReference
1	1 = Encoder 1: 2. reference markers crossed
2	1 = Encoder 2: 1. reference markers crossed
3	1 = Encoder 2: 2. reference markers crossed
4	0 = Transmitter ready for new data transfer 1 = Transmitter is occupied
5	0 = no extension module with sensor 5 / 6 available 1 = no extension module with sensor 5 / 6 available
6	0 = no extension module for external I/O available 1 = no extension module for external I/O available
7	0 = no extension module with ADC available 1 = no extension module with ADC available
8 – 15	Version FPGA

Table 30: State

Note for bit 4: Internal use. The IF card requires more time for sending commands to the sensor than the MEDAQLib to the IF card. With this bit the MEDAQLib checks if the IF card is ready for further applications.

Note for bit 5, 6, 7: Internal use. Displays if the IF2008E is connected. Commands for querying the bits: Is_Channel56Available, Is_ADCAvailable or IS_DigitalOAvailable.

5.15 Input

Base addr. + 26h (read access only)

Bit	Function
0	1 = ext. Input IN 1 active
1	1 = ext. Input IN 2 active
2	1 = ext. Input IN 3 active
3	1 = ext. Input IN 4 active
4	1 = RxD input on the sensor input 1 active
5	1 = RxD input on the sensor input 2 active
6	1 = RxD input on the sensor input 3 active
7	1 = RxD input on the sensor input 4 active
8	1 = RxD input on the sensor input 5 active
9	1 = RxD input on the sensor input 6 active
8 – 15	remarked

Table 31: Input

Note for bit 0 to 3: Internal use. Displays if the digital inputs are High or Low Command: Get_DigitalInValue.

Note for bit 4 to 9: Internal use. Displays if the RxD inputs are High or Low Command: Get_RxDValue.

5.16 Output Register

Base addr. + 2Eh (write and read access)

Bit	Function	Output Signal
0	0 = OUT 1 OFF Optocoupler blocked ¹⁾ 1 = OUT 1 ON Optocoupler conductive	Output 1 = High Output 1 = Low //Set_DigitalOutValue respect. Get_DigitalOutValue
1	0 = OUT 2 OFF Optocoupler blocked ¹⁾ 1 = OUT 2 ON Optocoupler conductive	Output 2 = High Output 2 = Low
2	0 = OUT 3 OFF Optocoupler blocked ¹⁾ 1 = OUT 3 ON Optocoupler conductive	Output 3 = High Output 3 = Low
3	0 = OUT 4 OFF Optocoupler blocked ¹⁾ 1 = OUT 4 ON Optocoupler conductive	Output 4 = High Output 4 = Low
4	0 = TxD 1 inactive 1 = TxD 1 active	TxD 1+ = High TxD 1- = Low TxD 1+ = Low TxD 1- = High //Set_TxDValue respect. Get_TxDValue
5	0 = TxD 2 inactive 1 = TxD 2 active	TxD 2+ = High TxD 2- = Low TxD 2+ = Low TxD 2- = High
6	0 = TxD 3 inactive 1 = TxD 3 active	TxD 3+ = High TxD 3- = Low TxD 3+ = Low TxD 3- = High
7	0 = TxD 4 inactive 1 = TxD 4 active	TxD 4+ = High TxD 4- = Low TxD 4+ = Low TxD 4- = High
8	0 = TxD 5 inactive ¹⁾ 1 = TxD 5 active	TxD 5+ = High TxD 5- = Low TxD 5+ = Low TxD 5- = High
9	0 = TxD 6 inactive ¹⁾ 1 = TxD 6 active	TxD 6+ = High TxD 6- = Low TxD 6+ = Low TxD 6- = High
10	0 = TRG 1 inactive 1 = TRG 1 active	TRG 1+ = Low TRG 1- = High TRG 1+ = High TRG 1- = Low //Set_TrgValue respect. Get_TrgValue
11	0 = TRG 2 inactive 1 = TRG 2 active	TRG 2+ = Low TRG 2- = High TRG 2+ = High TRG 2- = Low
12	0 = TRG 3 inactive 1 = TRG 3 active	TRG 3+ = Low TRG 3- = High TRG 3+ = High TRG 3- = Low
13	0 = TRG 4 inactive 1 = TRG 4 active	TRG 4+ = Low TRG 4- = High TRG 4+ = High TRG 4- = Low
14	0 = TRG 5 inactive ¹⁾ 1 = TRG 1 active	TRG 5+ = Low TRG 5- = High TRG 5+ = High TRG 5- = Low
15	0 = TRG 6 inactive ¹⁾ 1 = TRG 6 active	TRG 6+ = Low TRG 6- = High TRG 6+ = High TRG 6- = Low

Table 32: Output register

Please note:

For all outputs more signal sources are available. Bits listed above are only connected through in case that the appropriate mode is set (see table 33 on page 22: mode opto- and TxD outputs).

¹⁾ Expansion Board only

5.17 Mode Opto- and TxD Outputs

Base addr. + 30h (write and read access)

Bit	Function		
0 and 1	Bit 1	Bit 0	Function
	0	0	Output 1 connects with addr. 2Eh bit 0 //Set_DigitalOutSource respectively Get_DigitalOutSource
	0	1	Output 1 connects with timer 1 pulse width
	1	0	Output 1 connects with timer 2 pulse width
	1	1	Output 1 connects with timer 3 pulse width
2 and 3	Bit 3	Bit 2	Function
	0	0	Output 2 connects with addr. 2Eh bit 1
	0	1	Output 2 connects with timer 1 pulse width
	1	0	Output 2 connects with timer 2 pulse width
	1	1	Output 2 connects with timer 3 pulse width
4 and 5	Bit 5	Bit 4	Function
	0	0	Output 3 connects with addr. 2Eh bit 2
	0	1	Output 3 connects with timer 1 pulse width
	1	0	Output 3 connects with timer 2 pulse width
	1	1	Output 3 connects with timer 3 pulse width
6 and 7	Bit 7	Bit 6	Function
	0	0	Output 4 connects with addr. 2Eh bit 3
	0	1	Output 4 connects with timer 1 pulse width
	1	0	Output 4 connects with timer 2 pulse width
	1	1	Output 4 connects with timer 3 pulse width
8	0 = TxD 1 connects with transmitter 1 = TxD 1 connects with addr. 2Eh bit 4 //Set_TxDSource respectively Get_TxDSource		
9	0 = TxD 2 connects with transmitter 1 = TxD 2 connects with addr. 2Eh bit 5		
10	0 = TxD 3 connects with transmitter 1 = TxD 3 connects with addr. 2Eh bit 6		
11	0 = TxD 4 connects with transmitter 1 = TxD 4 connects with addr. 2Eh bit 7		
12	0 = TxD 5 connects with transmitter 1 = TxD 5 connects with addr. 2Eh bit 8		
13	0 = TxD 6 connects with transmitter 1 = TxD 6 connects with addr. 2Eh bit 9		
14 - 15	remarked		

Table 33: Mode Opto- and TxD Outputs

Please note:

The outputs 1 to 4 are only available for the IF2008E.

5.18 Mode Trigger Outputs

Base addr. + 32h (write and read access)

Configures the six trigger outputs, command in the MEDAQLib is Set_TrgSource.

Bit	Function		
0 and 1	Bit 1	Bit 0	Function
	0	0	Trigger 1 connects with addr. 2Eh bit 10
	0	1	Trigger 1 connects with timer 1 pulse width
	1	0	Trigger 1 connects with timer 2 pulse width
	1	1	Trigger 1 connects with timer 3 pulse width
2 and 3	Bit 3	Bit 2	Function
	0	0	Trigger 2 connects with addr. 2Eh bit 11
	0	1	Trigger 2 connects with timer 1 pulse width
	1	0	Trigger 2 connects with timer 2 pulse width
	1	1	Trigger 2 connects with timer 3 pulse width
4 and 5	Bit 5	Bit 4	Function
	0	0	Trigger 3 connects with addr. 2Eh bit 12
	0	1	Trigger 3 connects with timer 1 pulse width
	1	0	Trigger 3 connects with timer 2 pulse width
	1	1	Trigger 3 connects with timer 3 pulse width
6 and 7	Bit 7	Bit 6	Function
	0	0	Trigger 4 connects with addr. 2Eh bit 13
	0	1	Trigger 4 connects with timer 1 pulse width
	1	0	Trigger 4 connects with timer 2 pulse width
	1	1	Trigger 4 connects with timer 3 pulse width
8 and 9	Bit 9	Bit 8	Function
	0	0	Trigger 5 connects with addr. 2Eh bit 14
	0	1	Trigger 5 connects with timer 1 pulse width
	1	0	Trigger 5 connects with timer 2 pulse width
	1	1	Trigger 5 connects with timer 3 pulse width
10 and 11	Bit 11	Bit 10	Function
	0	0	Trigger 6 connects with addr. 2Eh bit 15
	0	1	Trigger 6 connects with timer 1 pulse width
	1	0	Trigger 6 connects with timer 2 pulse width
	1	1	Trigger 6 connects with timer 3 pulse width

Bit	Function			
12 – 14	Bit 14	Bit 13	Bit 12	Latch Source
	0	0	0	Hardware latch blocked
	0	0	1	Timer 1
	0	1	0	Timer 2
	0	1	1	Timer 3
	1	0	0	Sensor channel 1
	1	0	1	Sensor channel 2
	1	1	0	Sensor channel 3
1	1	1	Sensor channel 4	
15	remarked			

Table 34: Mode trigger outputs

Please note:

By means of bits 12-14 a latch source can be selected. The trigger process of the external inputs (IN1-4) and RxD input (sensor 1-6) allows recording the results synchronously to the FIFO.

The command in the MEDAQLib is `Set_DigitalLatchSource`.

5.19 ADC Control Register

Defining bit 0 to 7, when acquiring and evaluating an AD value in the FIFO. The synchronisation can be effected using a timer, a sensor cable or an pulse on the digital input IN1 ... IN4. Therefore an external triggering is possible due to the digital inputs.

Base addr. + 34h (write and read access)

Bit 3	Bit 2	Bit 1	Bit 0	Conversion Source ADC1
Bit 7	Bit 6	Bit 5	Bit 4	Conversion Source ADC2
0	0	0	0	Hardware converter blocked
0	0	0	1	Timer 1
0	0	1	0	Timer 2
0	0	1	1	Timer 3
0	1	0	0	Sensor channel 1
0	1	0	1	Sensor channel 2
0	1	1	0	Sensor channel 3
0	1	1	1	Sensor channel 4
1	0	0	0	Sensor channel 5
1	0	0	1	Sensor channel 6
1	0	1	0	IN 1 (IF2008E/ I/O only)
1	0	1	1	IN 2 (IF2008E/ I/O only)
1	1	0	0	IN 3 (IF2008E/ I/O only)
1	1	0	1	IN 4 (IF2008E/ I/O only)
1	1	1	0	remarked
1	1	1	1	remarked

Table 35: ADC control register bit 0-7

Bit	Function
8	0 = ADC1 data output binary 2-complement 1 = ADC 1 data output binary not converted
9	0 = ADC2 data output binary 2-complement 1 = ADC2 data output binary not converted
10 – 15	remarked

Table 36: ADC control register bit 8-15

Note for bit 8 and 9: Internal use. Function is not used in the MEDAQLib. The MEDAQLib cannot evaluate the switch setting for the analogue sections.

Analog Input				Digital Output	
0 – 5 V	0 – 10 V	+/-5 V	+/-10 V	Binary 2-complement	Binary not converted
+4.99 V	+9.99 V	+4.99 V	+9.99 V	7FFF	FFFF
2.5 V	5 V	0 V	0 V	0000	8000
+2.499 V	+4.999 V	-153 μ V	-305 μ V	FFFF	7FFF
0 V	0 V	-5 V	-10 V	8000	0000

Table 37: ADC converting result

5.20 Parity Enable Register

Base addr. + 36 0(write access)

Bit	Function
0	0 = Parity bit for sensor channel 1 blocked 1 = Parity bit for sensor channel 1 released (even parity only)
1	0 = Parity bit for sensor channel 2 blocked 1 = Parity bit for sensor channel 2 released (even parity only)
2	0 = Parity bit for sensor channel 3 blocked 1 = Parity bit for sensor channel 3 released (even parity only)
3	0 = Parity bit for sensor channel 4 blocked 1 = Parity bit for sensor channel 4 released (even parity only)
4	0 = Parity bit for sensor channel 5 blocked 1 = Parity bit for sensor channel 5 released (even parity only)
5	0 = Parity bit for sensor channel 6 blocked 1 = Parity bit for sensor channel 6 released (even parity only)
6-15	remarked

Table 38: Parity enable register

In the case that a sensor e.g. a time-of-flight sensor which data protocol uses the parity bit is chosen, the MEDAQLib activates the corresponding parity register automatically.

5.21 Parity Error Register

Base addr. + 36h (read access)

Bit	Function
0	1 = parity error sensor channel 1
1	1 = parity error sensor channel 2
2	1 = parity error sensor channel 3
3	1 = parity error sensor channel 4
4	1 = parity error sensor channel 5
5	1 = parity error sensor channel 6
6 – 15	remarked

Table 39: Parity error register

6 Recommendation Regarding Cabling

6.1 Sensor ILD1302 and ILD1402

Pin X1/X2 IF2008A Pin X1 IF2008E	Signal	ILD 1302, ILD1402		Signal Sensor
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	4		RxD-
2	Sensor 1 TxD+	3		RxD+
3	Sensor 1 RxD-	6		TxD-
4	Sensor 1 RxD+	5		TxD+
5	Power supply 0 V	12	12	GND
6	Sensor 1 TRG+	9		TeachIn
7	Sensor 1 TRG-	NC	NC	
8	Sensor 2 TRG+		9	TeachIn
9	Sensor 2 TRG-	NC	NC	
10	Power supply +24 V	7	7	+UB
11	Sensor 2 TxD-		4	RxD-
12	Sensor 2 TxD+		3	RxD+
13	Sensor 2 RxD-		6	TxD-
14	Sensor 2 RxD+		5	TxD+
15	GND (galvanic isolation to PC-GND)	12	12	GND

Table 40: Sensor cabling ILD1302 and ILD1402

6.2 Sensor ILD1700

Pin X1/X2 IF2008A Pin X1 IF2008E	Signal	ILD1700		Signal Sensor
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	11		RxD-
2	Sensor 1 TxD+	12		RxD+
3	Sensor 1 RxD-	2		TxD-
4	Sensor 1 RxD+	1		TxD+
5	Power supply 0 V	6	6	GND
6	Sensor 1 TRG+	3		TRG+
7	Sensor 1 TRG-	4		TRG-
8	Sensor 2 TRG+		3	TRG+
9	Sensor 2 TRG-		4	TRG-
10	Power supply +24 V	5	5	+UB
11	Sensor 2 TxD-		11	RxD-
12	Sensor 2 TxD+		12	RxD+
13	Sensor 2 RxD-		2	TxD-
14	Sensor 2 RxD+		1	TxD+
15	GND (galvanic isolation to PC-GND)	6	6	GND

Table 41: Sensor cabling ILD1700

6.3 Sensor ILD2200

Pin X1/X2 IF2008A Pin X1 IF2008E	Signal	ILD2200		Signal Sensor
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	24		RxD-
2	Sensor 1 TxD+	11		RxD+
3	Sensor 1 RxD-	10		TxD-
4	Sensor 1 RxD+	23		TxD+
5	Power supply 0 V	14	14	Supply ground
6	Sensor 1 TRG+	20		SyncIn+
7	Sensor 1 TRG-	NC		
8	Sensor 2 TRG+		20	SyncIn+
9	Sensor 2 TRG-		NC	
10	Power supply +24 V	1	1	+UB
11	Sensor 2 TxD-		24	RxD-
12	Sensor 2 TxD+		11	RxD+
13	Sensor 2 RxD-		10	TxD-
14	Sensor 2 RxD+		23	TxD+
15	GND (galvanic isolation to PC-GND)	7	7	SyncIn-

Table 42: Sensor cabling ILD2200

6.4 Sensor ILD2300

Pin X1/X2 IF2008A Pin X1 IF2008E	Signal	ILD2200		Signal Sensor
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	8		RxD-
2	Sensor 1 TxD+	7		RxD+
3	Sensor 1 RxD-	10		TxD-
4	Sensor 1 RxD+	9		TxD+
5	Power supply 0 V	2	2	Supply ground
6	Sensor 1 TRG+	5		SyncIn+
7	Sensor 1 TRG-	6		SyncIn-
8	Sensor 2 TRG+		5	SyncIn+
9	Sensor 2 TRG-		6	SyncIn-
10	Power supply +24 V	1	1	+UB
11	Sensor 2 TxD-		8	RxD-
12	Sensor 2 TxD+		7	RxD+
13	Sensor 2 RxD-		10	TxD-
14	Sensor 2 RxD+		9	TxD+
15				

Table 43: Sensor cabling ILD2300

6.5 Encoder Interface

Pin X3 IF2008A	Signal	1V _{ss} or RS422		TTL (single-ended)	
		Signal Encoder 1	Signal Encoder 2	Signal Encoder 1	Signal Encoder 2
1	Encoder 1 track A+	A+		A	
2	Encoder 1 track A-	A-		open	
3	Encoder 2 track A+		A+		A
4	Encoder 2 track A-		A-		open
5	VCC (+5 V)	+UB	+UB	+UB	+UB
6	Encoder 1 track B+	B+		B	
7	Encoder 1 track B-	B-		open	
8	Encoder 2 track B+		B+		B
9	Encoder 2 track B-		B-		open
10	GND	GND	GND	GND	GND
11	Encoder 1 track R+	R+		R	
12	Encoder 1 track R-	R-		open	
13	Encoder 2 track R+		R+		R
14	Encoder 2 track R-		R-		open
15	GND	GND	GND	GND	GND

Table 44: Encoder interface

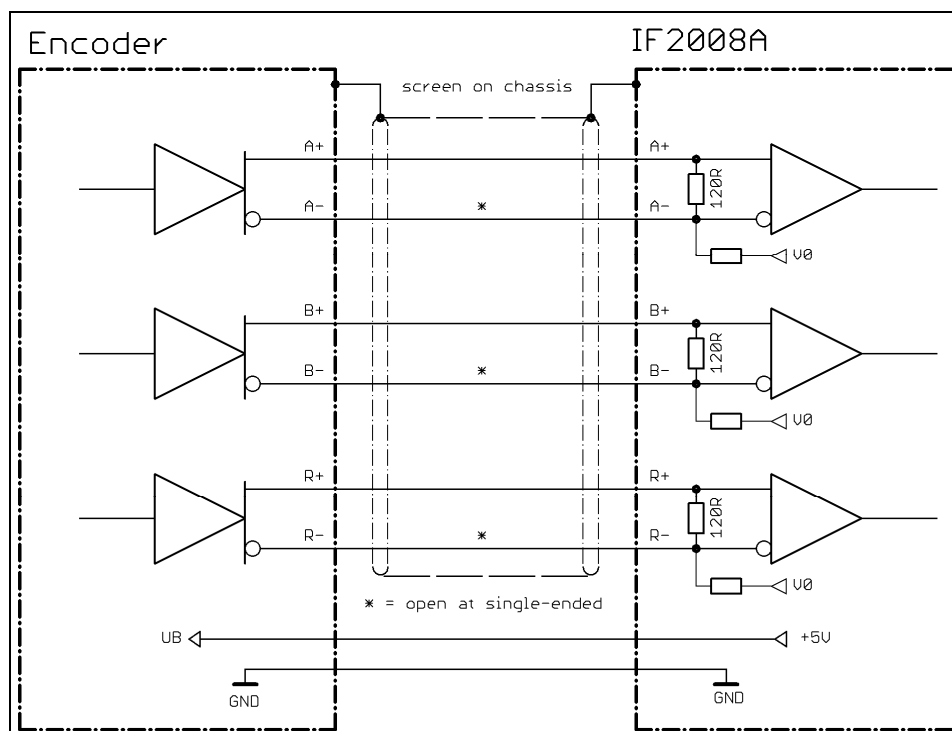


Image 6: Block diagram encoder interface

Please note:

Non-inverting inputs (A+, B+, R+) may not keep open. For example, if only the clock is used regarding the counter, the plus inputs have to be set on GND or VCC.
Not assigned negative inputs (A-, B-, R-) may not be connected with GND.

6.6 Optocoupler I/O

Pin X2 IF2008E	Signal
1	OUT 1
2	OUT 2
3	OUT 3
4	OUT 4
5	GND (galvanic isolation to PC-GND)
6	IN 1
7	IN 2
8	IN 3
9	IN 4

Table 45: Optocoupler I/O

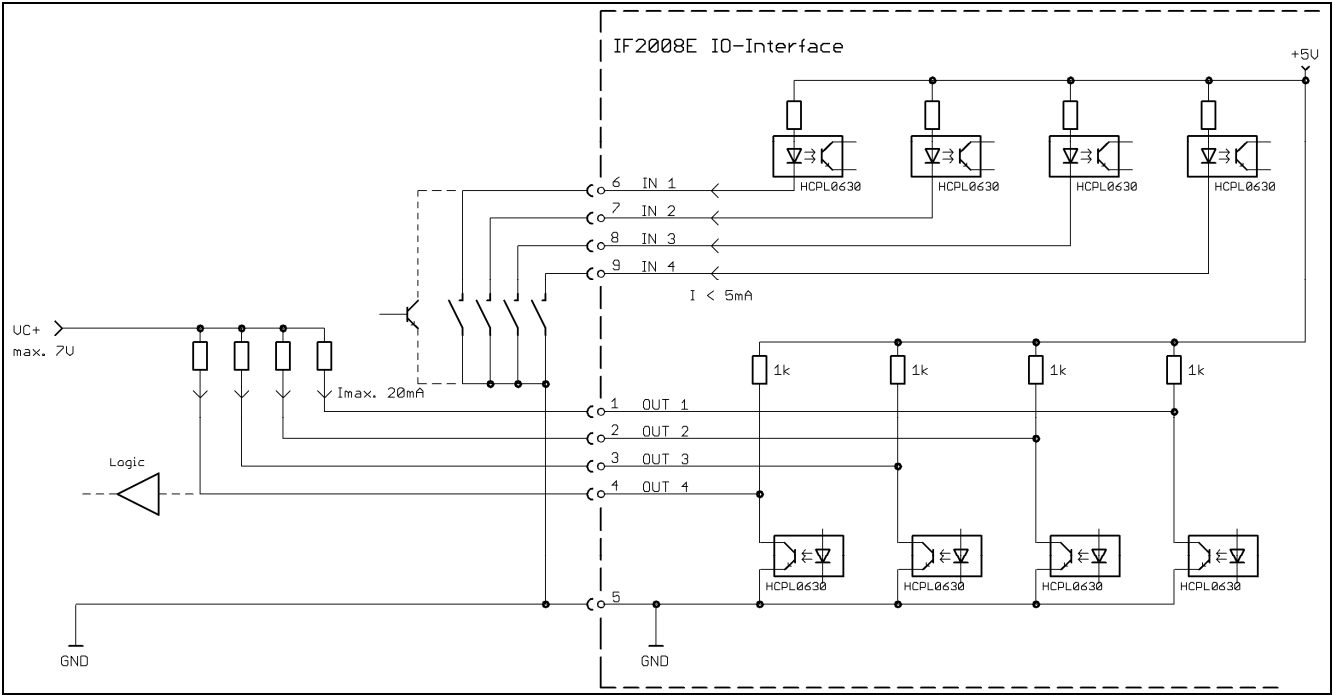


Image 7: Block diagram optocoupler I/O

7 Examples for Synchronisation, Triggering, Gating

Synchronisation = fast application (passive, only „listening“)

Triggering = slow application (active, command and answer)

The following examples show using the ILD1700 sensor as an example the possibilities for data acquisition.

7.1 Get a Measuring Value from the Sensor, Software-trigger

- SET_ERROROUTPUT
- GET_MEASVALUE: One measuring value or more.
- DATAAVAIL: One measuring value or more are available.
- TRANSFERDATA: Evaluates a measuring value from the ring buffer.

7.2 Hardware-Trigger

- SET_ERROROUTPUT: Sensor set in trigger mode, X = “2” or “3”.
- SET_SYNCMODE/TRIGGERMODE: Set the reaction of the sensor input to the flank or level
- Square pulse on the sensor input caused by e.g. the SPS or trigger output of the IF2008.
- DATAAVAIL: not absolutely necessary.
- TRANSFERDATA: Evaluates measuring value from the ring buffer the last value is given first. OR
- POLL: First in, first out, values are stored in the ring buffer. Function for control and regulation applications.

7.3 Software Gating (Gate) on the Sensor

- DAT_OUT_ON: The digital data output of the measuring values is activated
- TRANSFERDATA: Evaluates measuring values from the ring buffer, delivers the last given value first.
- DAT_OUT_OFF: Deactivates the digital data output of the measuring values.

7.4 Hardware Gating (Gate) on the Sensor

- SET_SYNCMODE/TRIGGERMODE: Set the reaction of the sensor input to low or high level.
- Create the level on the sensor input.
- TRANSFERDATA: Evaluates measuring values from the ring buffer, delivers the last given value first.

This example requires the functionality in the sensor.

7.5 Hardware Gating (Gate) with IF2008

- Data is continuously given by the sensor
- USE_GATE: Opens or blocks the FIFO.
- 5V TTL an IF2008: Data is acquired or blocked.
- CLEAR_BUFFERS: Deletes the ring buffer and the in-output buffer of the IF2008. Therefore, using decaying data is avoided.
- TRANSFERDATA: Evaluates the measuring value from the ring buffer, the last given value is given first.

7.6 Synchronised Measuring ValueEvaluation with Encoder and IF2008

Construction: Sensor on cable 1, encoder on channel 7 (first encoder)

- SensorID = CreateSensorInstance (SENSOR_ILD1700)
- SetParameterString (SensorID, "IP_Interface", "IF2008")
- OpenSensor (SensorID)
- SetParameterString (SensorID, "S_Command", "Get_Settings")
- SensorCommand (SensorID)

- EncoderID = CreateSensorInstance (PCI_CARD_IF2008)
- SetParameterString (EncoderID, "IP_Interface", "IF2008")
- SetParameterInt (EncoderID, "IP_ChannelNumber", 6)
- OpenSensor (EncoderID)
- SetParameterString (EncoderID, "S_Command", "Set_EncoderInterpolation")
- SetParameterInt (EncoderID, "SP_EncoderInterpolation", 0) // 0 = single evaluation
- SensorCommand (EncoderID)

- SetParameterString (EncoderID, "S_Command", "Set_EncoderLatchSource")
- SetParameterInt (EncoderID, "SP_EncoderLatchSource", 4) //4 = Sensor on channel 1, synchronised evaluation with ILD1700
- SensorCommand (EncoderID)

- SetParameterString (SensorID, "S_Command", "Clear_Buffers")
- SetParameterInt (SensorID, "SP_AllDevices", 1) // 1 = deletes all connected buffers of the unit
- SensorCommand (SensorID)

while (running)

```
{  
    TransferData (SensorID, rawData, scaledData, nbrValues, read)  
    TransferData (EncoderID, rawData, scaledData, nbrValues, read)  
    ...  
}
```

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